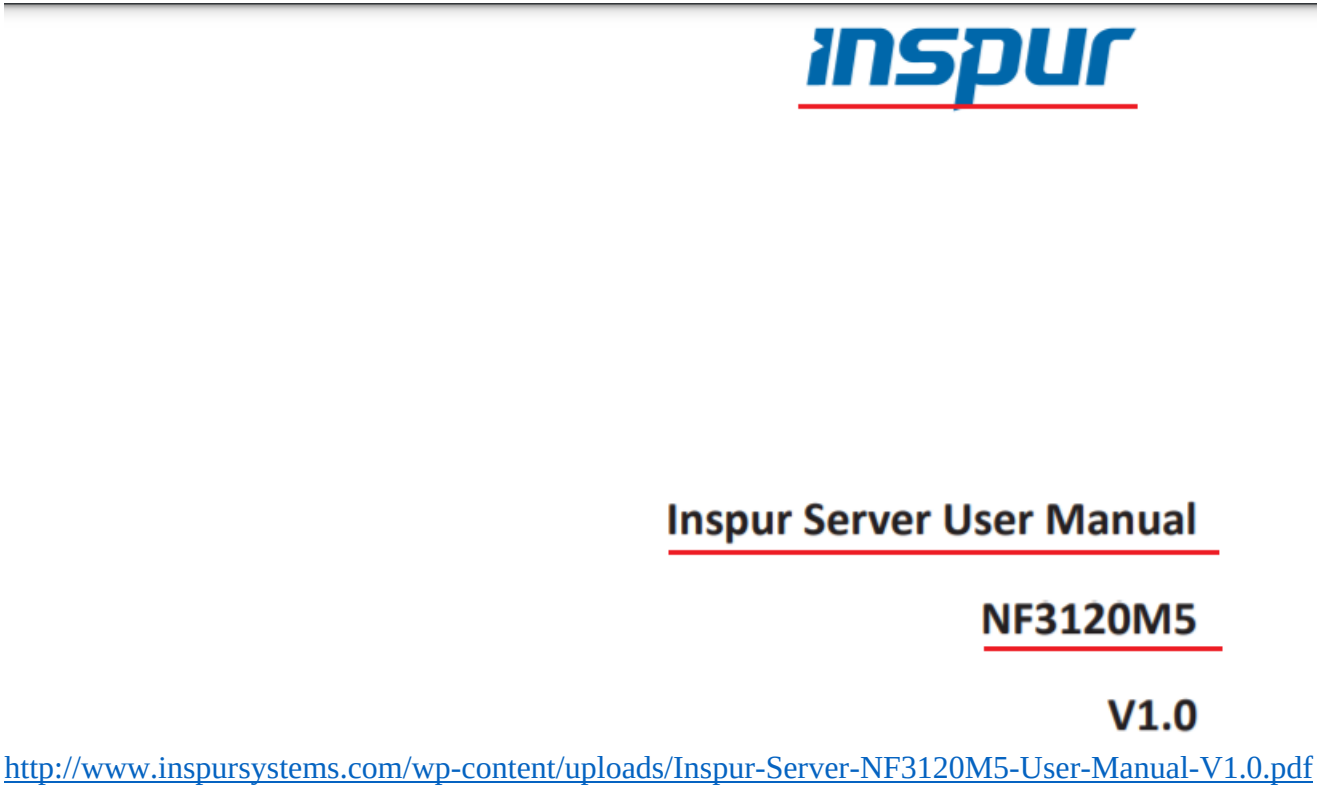
EXHIBIT B

US6603330	NF3120M5 (“The Accused Product”)
25. A method of programming a programmable digital circuit block, comprising the steps of:	The accused product discloses a method of programming a programmable digital circuit block (e.g., DDR 4 SDRAM).  http://www.inspursystems.com/wp-content/uploads/Inspur-Server-NF3120M5-User-Manual-V1.0.pdf

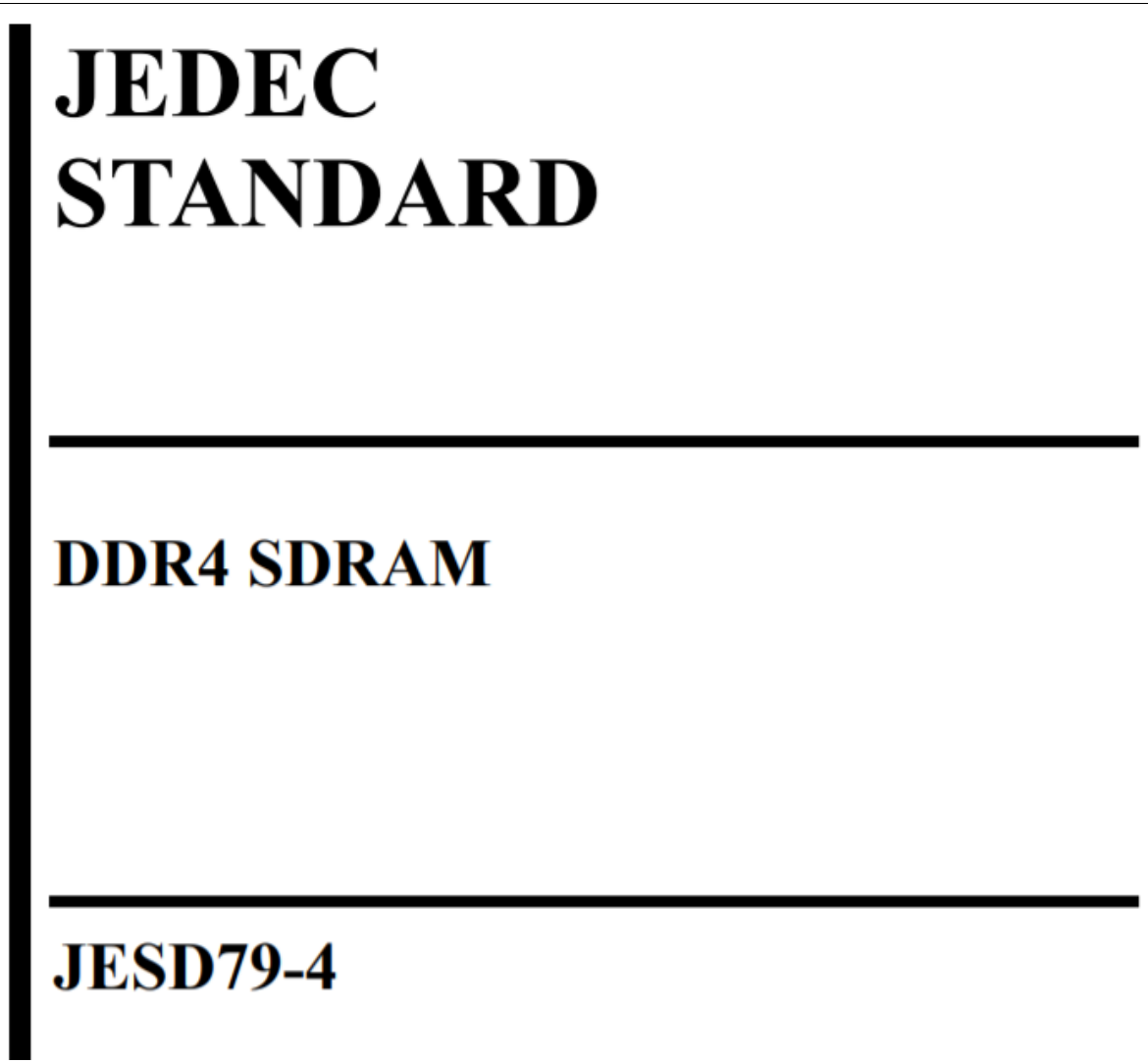
2.1 Overview

Inspur NF3120M5 is a one-socket E3 server with Intel® Xeon® scalable computing platform technology. It has powerful computing capacity, scalability and excellent RAS features. It provides basic computing and graphics performance, which is an ideal choice for small businesses, powerful mobile workstation, entry-level workstation, storage server, cloud workstation, media codec, edge computing and Internet of Things.

2.2 Features and Specifications

Processor	
Processor Type	1* new-generation Intel® Xeon® scalable processor (up to 95W)
Chipset	
Chipset Type	Intel® C242/C246 chipset
Memory	
Memory Type	DDR4 w/ECC UDIMM, 2666MHz
Memory Slot Qty	4
Total Memory Capacity	Supports up to 128GB (32G per memory module)
I/O	

http://www.inspursystems.com/wp-content/uploads/Inspur-Server-NF3120M5-User-Manual-V1.0.pdf

	 Source: DDR 4 standard
a) loading a plurality of configuration data corresponding to any one of a	The accused product discloses loading a plurality of configuration data (e.g., bits A1, A0) corresponding to any one of a plurality of predetermined digital functions (e.g., read/write operations of fixed burst

plurality of predetermined digital functions into a configuration register of said programmable digital circuit block; and	length of BC8 or BC4; read/write operations of on-the-fly burst length of BC8 or BC4) into a configuration register (e.g., Mode register MR0) of said programmable digital circuit block (e.g., DDR 4 SDRAM). 3.4.1 Programming the mode registers For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array Source: DDR 4 standard

3.5 Mode Register

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	RFU	0 = must be programmed to 0 during MRS
A11:A9	WR and RTP[2, 3]	Write Recovery and Read to Precharge for auto precharge(see Table 1)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A6:A4,A2	CAS Latency[4]	(see Table 2)

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Address	Operating Mode	Description
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

Source: DDR 4 standard

b) configuring said programmable digital circuit block to perform any one of said plurality of predetermined digital functions based on said configuration data, wherein said steps a) and b) are dynamically performed, and wherein said programmable digital circuit block includes a data register for storing data to facilitate performing any one of said plurality of predetermined digital functions.	The accused product discloses configuring said programmable digital circuit block (e.g., DDR 4 SDRAM) to perform any one of said plurality of predetermined digital functions (e.g., read/write operations of fixed burst length of BC8 or BC4; read/write operations of on-the-fly burst length of BC8 or BC4) based on said configuration data (e.g., bits A1, A0), wherein said steps a) and b) are dynamically performed (e.g., dynamically performed based on MRS command), and wherein said programmable digital circuit block includes a data register (e.g., register storing) for storing data to facilitate performing any one of said plurality of predetermined digital functions. The data is bit A12. It is used according to the configuration data MR0 [A1, A0] to facilitate performing any one of the predetermined digital functions. For instance, if MR0[A1, A0] indicates on-the-fly (OTF) burst length, then A12 determines if the OTF burst length is BC4 or 8, and hence facilitates performing the read/write operations of OTF burst length BC4 or 8. 3.4.1 Programming the mode registers For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array Source: DDR 4 standard

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A13	RFU	0 = must be programmed to 0 during MRS
A12	RFU	0 = must be programmed to 0 during MRS
A11:A9	WR and RTP[2, 3]	Write Recovery and Read to Precharge for auto precharge(see Table 1)
A8	DLL Reset	0 = NO 1 = Yes
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Source: DDR 4 standard

Table 16 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address(RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

	Source: DDR 4 standard A12 / BC_n | Input | Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details. Source: DDR 4 standard